DEVELOPMENT OF "STITCH" SUPER-GTOS FOR PULSED POWER

Heather O'Brien, Aderinto Ogunniyi, Charles J. Scozzie
U.S. Army Research Laboratory, 2800 Powder Mill Road
Adelphi, MD 20783 USA
William Shaheen
Berkeley Research Associates, 6551 Mid Cities Ave
Beltsville, MD 20705 USA
Victor Temple
Silicon Power Corp., 958 Main St., Suite A
Clifton Park, NY 12065 USA

Abstract

Newly designed, high-power silicon gate turn-off thyristors are being evaluated to satisfy the U. S. Army's need for compact, lightweight pulse switches. Following the successful demonstration of a 3.5 cm^2 silicon Super-GTO, Silicon Power Corporation re-designed the emitter layout and increased the device footprint to create a switch optimized for use in high-current, wide-pulse applications. The 7 cm^2 silicon "Stitch" Super-GTO was developed to block 7 kV. The 2x increase in die size actually results in a 2.5x increase in active area because a portion of chip area that was previously taken up by perimeter high voltage termination is now used for conduction. The Super-GTOs were evaluated at the Army Research Laboratory in a low-inductance pulse-forming network. Pulse current was successfully stepped up as high as 35 kA, corresponding to a current density of 5 kA/cm^2 over the chip's footprint. This corresponds to 7 kA/cm^2 over the active emitter area, when the edge termination is excluded. Compared to Silicon Power's original device, the new larger component conducted 40% higher current density. The 35 kA current pulse had a width of 125 µs and an I^2t of 9.2 $x10^4$ A^2s. The 10-90% rise of the current pulse was 2.4 kA/µs, and the maximum on-state forward conduction drop was 28 V. Given good processing and packaging yields, this larger Stitch Super-GTO can greatly reduce the size of high current pulse switches.

I. INTRODUCTION

To support the development of power-dense switches for mobile platforms, the U.S. Army Research Laboratory (ARL) is researching the capabilities of new solid-state switch designs. Solid-state pulsed power switches offer the advantages of longer shot life, higher repetition rates, increased durability and reliability, smaller volume, and more flexibility in operating voltage and current ranges. Silicon Super-GTO (SGTO) designs, originated by Silicon Power (SPCO), are being pursued because of the high level of performance SGTOs have demonstrated as part of larger-scale switches for pulse vehicle applications. These devices have been switched at higher current densities per package volume, higher dI/dt per silicon area, and faster recovery times than wafer-scale silicon thyristors [1, 2].

The Army Research Laboratory is working with Silicon Power to further improve the pulse performance by increasing the current density at the individual SGTO chip level. SGTOs can then be packages in series and parallel configurations to reach the high voltages and high currents required by pulsed power systems. If new SGTO designs continue to show improved power densities and reliable performance for pulse applications, they may will become critical components for future Army vehicle systems.

II. DESIGN EVOLUTION

A. Previous SGTO Designs

The original silicon Super-GTO was designed for fast turn-on and high dI/dt. The prefix "Super" was used to denote a thin chip with a multi-zone high voltage termination and a cell-based gate layout [3]. The silicon footprint was 3.5 cm^2 with an active (mesa) area of 2.0 cm^2. Pulse evaluations completed at ARL suggested current crowding occurred at a peak current density of 5 kA/cm^2 for a 125 µs-wide pulse. As a result, Silicon Power took steps to improve lateral current flow and reduce on-state resistance by doubling the percentage of SGTO emitter area and changing the metal pattern (Fig. 1). This newer design, dubbed the Super-12 SGTO, was switched at 20% higher pulse current and 5 V lower voltage drop for the same size chip (Fig. 2). The Super-12 design matched the other turn-on, dI/dt, and dV/dt immunity capabilities of the original standard GTO design.

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14. ABSTRACT

Newly designed, high-power silicon gate turn-off thyristors are being evaluated to satisfy the U. S. Armys need for compact, lightweight pulse switches. Following the successful demonstration of a 3.5 cm2 silicon Super- GTO, Silicon Power Corporation re-designed the emitter layout and increased the device footprint to create a switch optimized for use in high-current, wide-pulse applications. The 7 cm2 silicon Stitch Super-GTO was developed to block 7 kV. The 2x increase in die size actually results in a 2.5x increase in active area because a portion of chip area that was previously taken up by perimeter high voltage termination is now used for conduction. The Super-GTOs were evaluated at the Army Research Laboratory in a low-inductance pulse-forming network. Pulse current was successfully stepped up as high as 35 kA, corresponding to a current density of 5 kA/cm2 over the chips footprint. This corresponds to 7 kA/cm2 over the active emitter area, when the edge termination is excluded. Compared to Silicon Powers original device, the new larger component conducted 40% higher current density. The 35 kA current pulse had a width of 125 ìs and an I2t of 9.2 x104 A2s. The 10-90% rise of the current pulse was 2.4 kA/ìs, and the maximum on-state forward conduction drop was 28 V. Given good processing and packaging yields, this larger Stitch Super- GTO can greatly reduce the size of high current pulse switches.

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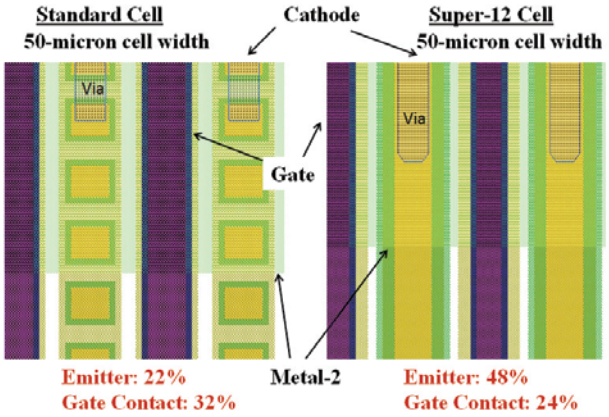

Figure 1. SGTO design changes incorporated in the more-capable Super-12 and Stitch devices. The percentage of emitter area was increased, and the metal pattern was modified.

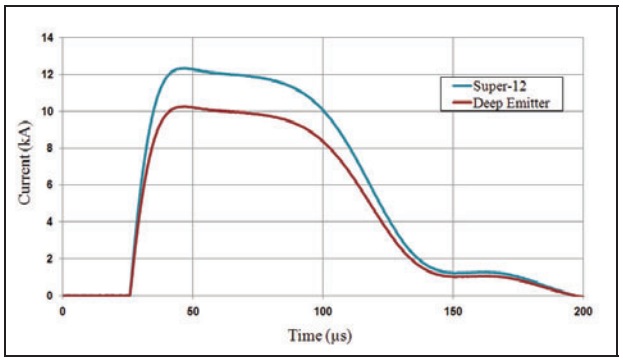

Figure 2. The emitter layout for the Super-12 SGTO enabled 20% higher pulse current (and current density) than the original layout.

B. Stitch SGTO Design

The Stitch SGTO incorporates the design modifications of the Super-12 but is fabricated in a device footprint of twice the area, essentially "stitching" two Super-12 SGTOs together. In doubling the chip layout to 7 cm^2, the active (mesa) area actually scales up by a factor of 2.5x because a smaller percentage of SGTO area is taken up by the edge termination (Fig. 3). The first few Stitch SGTOs were individually packaged at Silicon Power for pulse evaluation at ARL. Silicon Power's thinPak lids were fabricated in a larger size to facilitate connection to the gate-cathode surface of the SGTOs [4]. Each device was attached to a copper-moly base plate and encased in epoxy (Fig. 4).

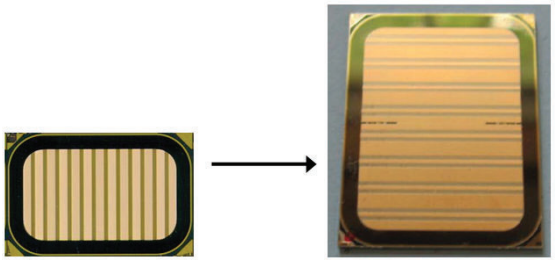

Figure 3. The Stitch SGTO (above right) is twice the footprint of the previous SGTOs, but 2.5x the active area.

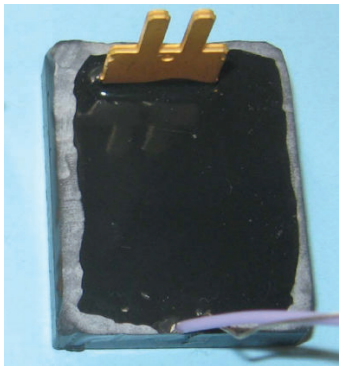

Figure 4. Individually packaged Stitch SGTO with high-current cathode tab protruding from the top and low-current gate wires at the bottom.

C. Static Characteristics

The gates of the SGTOs were initially evaluated to determine their forward and reverse characteristics. In the forward direction, gate current began flowing at 0.6 V, conducting 1 A at 0.7 V (Fig. 5). In the reverse direction, the gate exhibited a zener characteristic at -17 V (Fig. 6). These gate voltage values were similar to those of the previous silicon SGTO designs. The first set of Stitch SGTOs was only evaluated up to 4 kV for off-state blocking voltage. The epilayer and termination should handle up to 7 kV blocking, but since this was the first attempt to package these larger devices, and since the pulse circuit was designed to operate at a lower voltage, only 4 kV blocking capability was necessary.

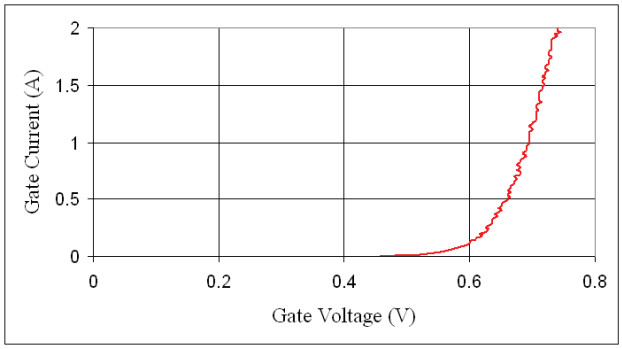

Figure 5. Forward gate characteristic of the SGTO exhibited a 0.7 V drop at 1 A of gate current.

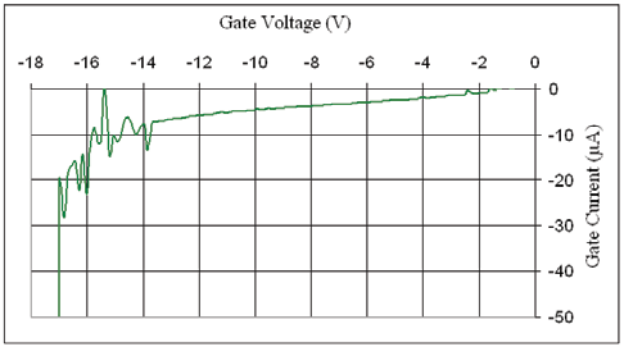

Figure 6. Reverse gate characteristic of the SGTO exhibited a zener characteristic at -17 V.

III. PULSE EVALUATIONS

A. Evaluation Methods

The Stitch SGTO was evaluated as a pulse switch to discharge stored capacitive energy into a resistive load. The circuit used was a relatively low-inductance pulse forming network (Fig. 7) that was previously used to demonstrate capabilities of larger solid-state switches, as well as the standard and Super-12 SGTO chips. By evaluating several different switch designs under the same pulse current conditions, direct comparisons were made between the capabilities of these devices. The Stitch SGTO was mounted to a larger copper base plate, which then served as the anode connection in the circuit. Other small copper plates were used to clamp to the cathode tab (Fig. 8). To trigger the SGTO, a square pulse current of 1.9 A amplitude, 12 A/µs dI/dt, and 10 µs width was applied gate-to-cathode. This gate current was twice the amplitude of that used for the smaller silicon SGTOs, accounting for increased chip area.

The primary switching parameters evaluated in the pulse circuit were maximum peak pulse current, action (I^2t), dI/dt rise, and on-state voltage drop. The Stitch SGTO was expected to exhibit a higher pulse current density and have a lower on-state voltage drop based on the design changes made to the emitter and metallization layer. Because this was the first time this device design and package were being pulsed, care was taken to step the current up slowly and monitor voltage and current waveforms for any change from one pulse to the next one.

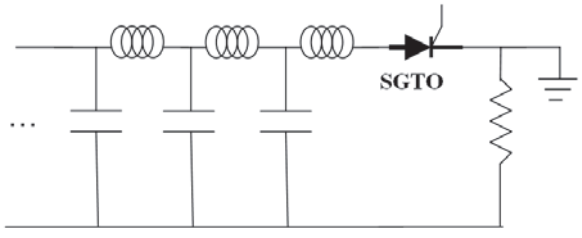

Figure 7. Schematic of the test circuit for the SGTO, with low inductance, low resistance, and 3 kJ capacitor storage.

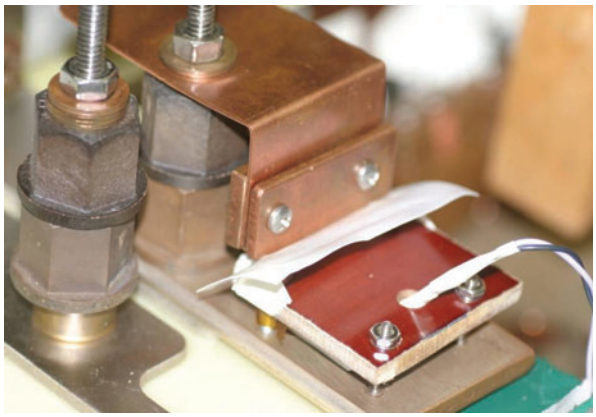

Figure 8. Stitch SGTO package clamped in pulse circuit. The SGTO was triggered to discharge a capacitor bank into a resistive load.

B. Results

The first Stitch SGTO was pulsed at increasing 1000-amp increments up to 35 kA (9.2 x10^4 A^2s) (Fig. 9). Seven pulses were completed at this level, during which the on-state voltage drop of the SGTO increased by 2 V. Based on experience, the increasing voltage drop can be associated with current crowding and hot spots in the device, which in turn lead to failure [5]. The SGTO completed one more pulse at a lower current amplitude before failing as a near short between the anode and cathode. The Stitch was expected to be able to switch at least 2.5-times the pulse current of the Super-12, because the Stitch's active area is 2.5-times that of the Super-12. The Stitch SGTO did exceed this expectation of >30 kA, but was possibly pushed too far at the 35 kA level. The operating level for this pulse shape is now predicted to be about 32 kA, or 6.4 kA/cm^2 over the active area. This current density was 7% higher than was demonstrated with the Super-12 design (Fig. 10). The 10-90% dI/dt of the current waveform was 2.4 kA/µs, as driven by the circuit topology and does not stress the maximum dI/dt capability of the SGTO device.

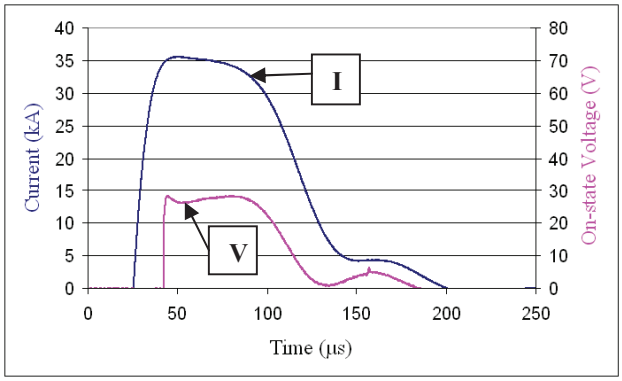

Figure 9. Peak pulse current (35 kA) and recorded anode-cathode voltage drop (28 V) for the SGTO. Voltage measurement was not introduced until 15 µs after initial trigger in order to capture a finer on-state measurement.

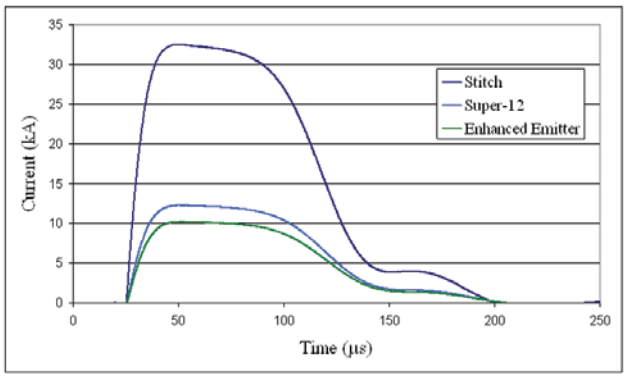

Figure 10. Stitch SGTO current shown at likely operating level of 32 kA. This is 7% higher current density than the smaller Super-12 design, and 28% higher current density than the older Enhanced Emitter SGTO design.

A second Stitch SGTO was installed in the circuit and switched in increments up to 21 kA, at which point the device unexpectedly failed during the pulse. Just as the current peaked, the package burst open causing a disconnect with the cathode tab. It is believed that either a 90-degree bend where the cathode tab met the topside of the SGTO, or a bad solder connection at that point, created a mechanical weak point that could not withstand the high pulse current. Upon further examination, the second SGTO still had a good gate and maintained high voltage blocking following the failure of the package; this suggests that the bursting of the package was solely related to how it was assembled. This failure highlights the challenges of developing high-voltage, high-current pulse switches for ever-shrinking volumes. Packaging research needs to progress in step with the development of the solid-state devices.

C. Further Testing

Following a review of the packaging techniques, additional individually packaged Stitch SGTOs will be delivered to ARL for pulse evaluation. They will be switched in the same pulse circuit but limited to a peak current of 30-32 kA and switched repetitively to evaluate the stability and reliability of the device. In the meantime, Silicon Power has assembled a module of four parallel Stitch SGTOs, similar to modules ARL has previously evaluated (Fig. 11) [1]. This module has undergone preliminary high current switching, and is expected to be capable of 120 kA.

Figure 11. Four-chip Stitch SGTO module designed for voltage blocking up to 7 kV and pulse current up to 120 kA.

IV. SUMMARY

A 7 cm^2 "Stitch" Super-GTO was designed and fabricated in silicon at twice the area of earlier Super-GTO devices. An increase in active area, in conjunction with modifications to the emitter and a metal layouts, enabled high-current pulsing above 30 kA. The maximum current switched was 35 kA, with a rise time of 2.4 kA/µs, an action of 9.2 x 10^4 A^2s, and an on-state voltage of 28 V. A weakness in the packaging was identified, and once that is resolved, more devices will be evaluated in order to determine if the Stitch is a suitable replacement or complement for smaller-area Super-GTOs in Army pulsed power applications.

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